FIG. 1

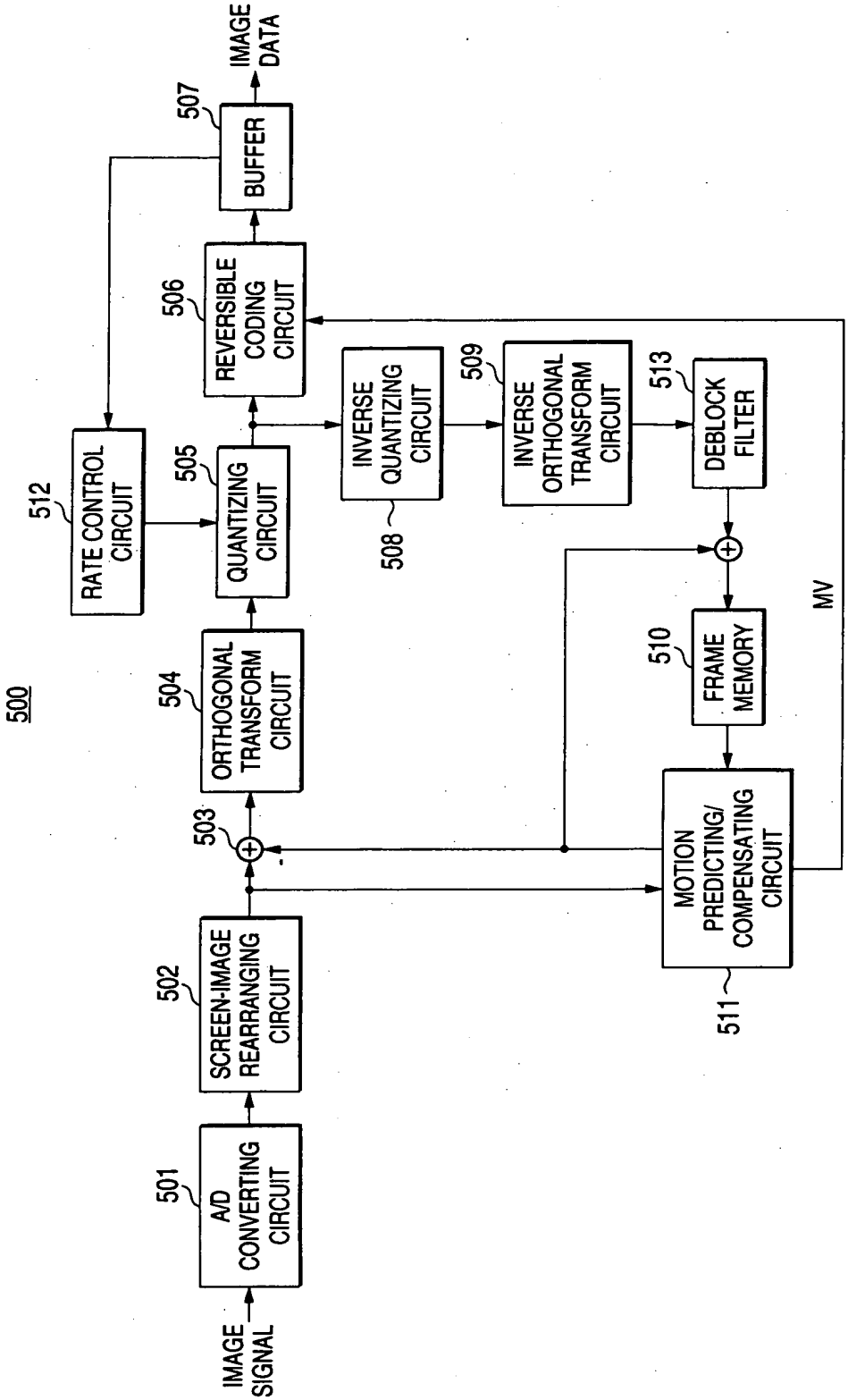

500
IMAGE SIGNAL
501
A/D CONVERTING CIRCUIT
502
SCREEN-IMAGE REARRANGING CIRCUIT
503
-
504
ORTHOGONAL TRANSFORM CIRCUIT
505
QUANTIZING CIRCUIT
506
REVERSIBLE CODING CIRCUIT
507
BUFFER
IMAGE DATA
508
INVERSE QUANTIZING CIRCUIT
509
INVERSE ORTHOGONAL TRANSFORM CIRCUIT
510
FRAME MEMORY
511
MOTION PREDICTING/ COMPENSATING CIRCUIT
512
RATE CONTROL CIRCUIT
513
DEBLOCK FILTER
MV

FIG. 2

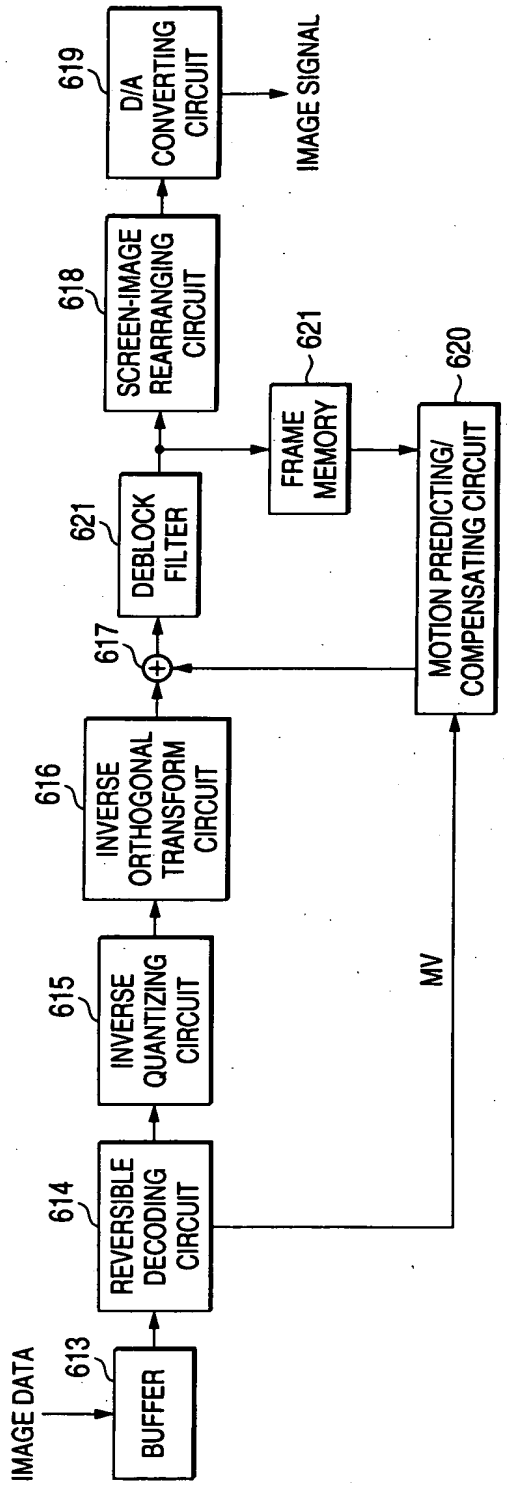

499
IMAGE DATA
613
BUFFER
614
REVERSIBLE DECODING CIRCUIT
615
INVERSE QUANTIZING CIRCUIT
616
INVERSE ORTHOGONAL TRANSFORM CIRCUIT
617
621
DEBLOCK FILTER
618
SCREEN-IMAGE REARRANGING CIRCUIT
619
D/A CONVERTING CIRCUIT
IMAGE SIGNAL
621
FRAME MEMORY
620
MOTION PREDICTING/ COMPENSATING CIRCUIT
MV

FIG. 3

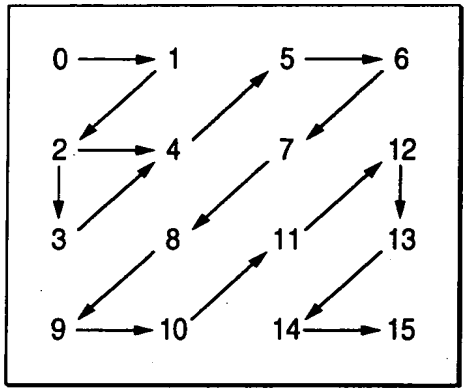


FIG. 4

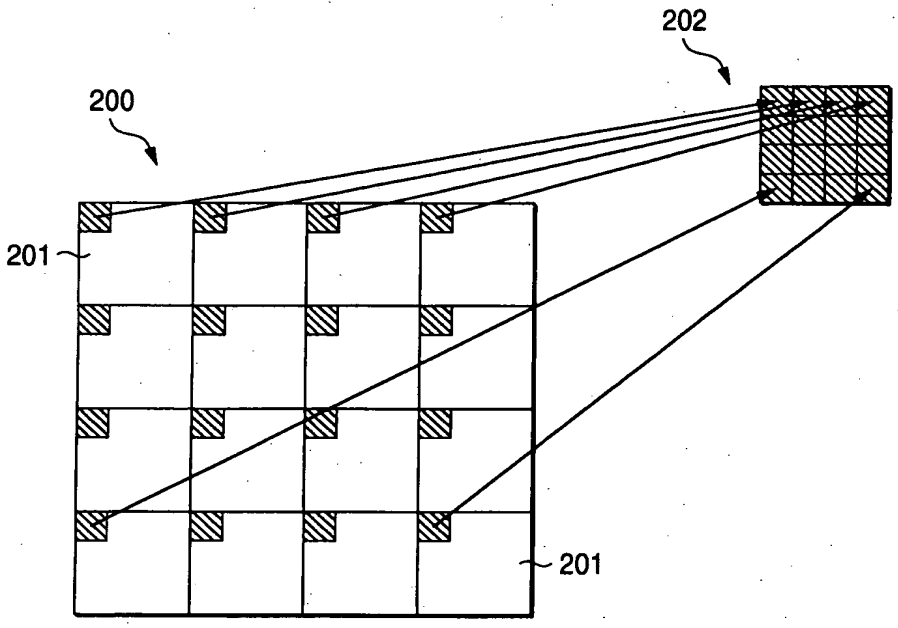


FIG. 5

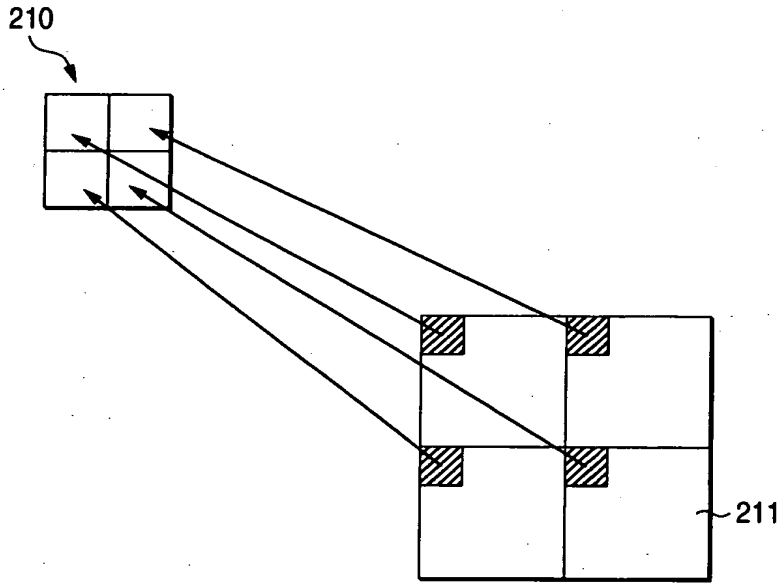


FIG. 6

QPY	< 30	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
QPC	= QPY	29	30	31	32	32	33	34	34	35	35	36	36	37	37	37	38	38	38	39	39	39	39

FIG. 7

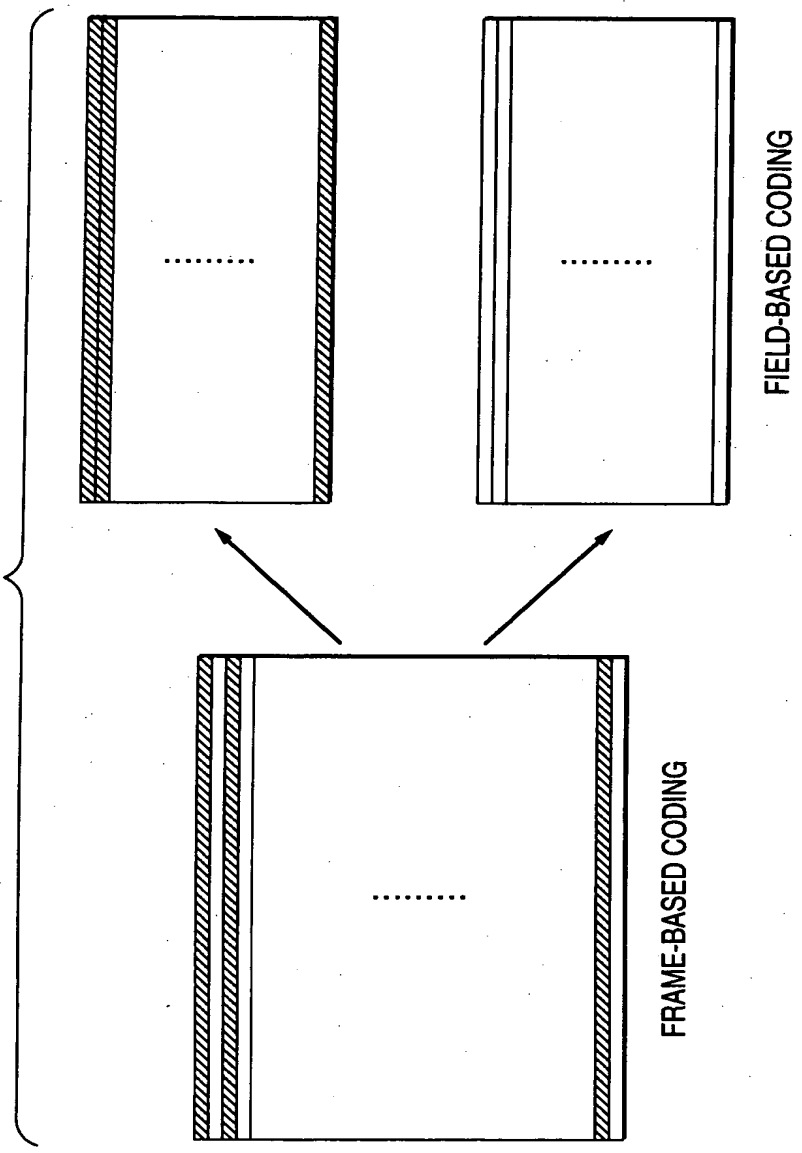


FIG. 8B

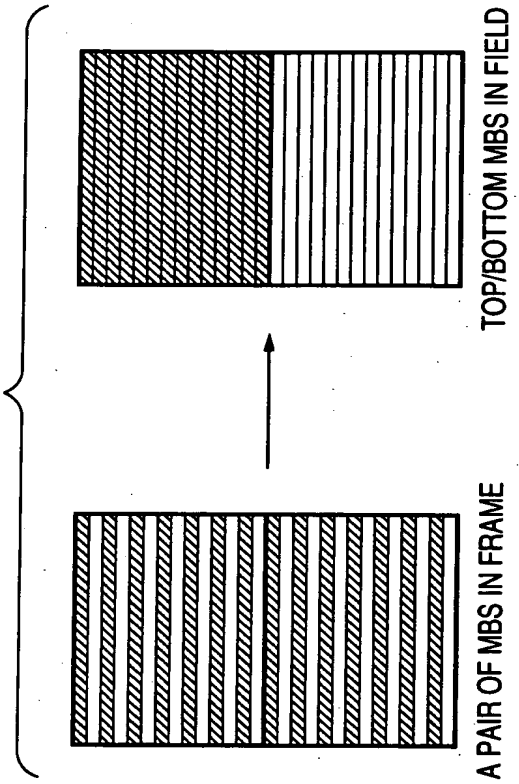


FIG. 8A

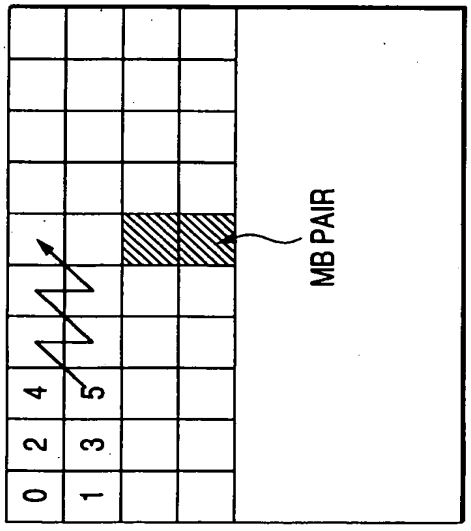


FIG. 9

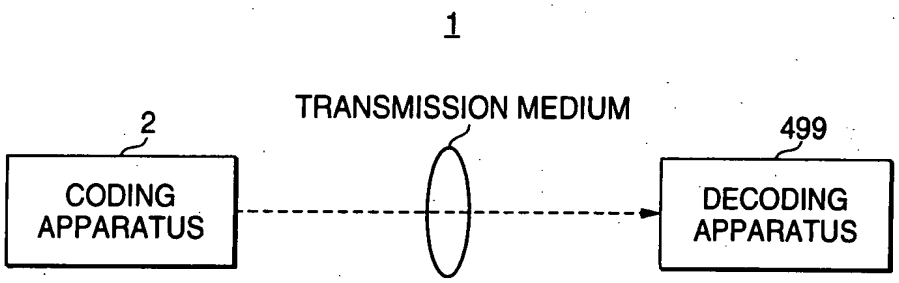

1
TRANSMISSION MEDIUM
2
499
CODING APPARATUS
DECODING APPARATUS

FIG. 10

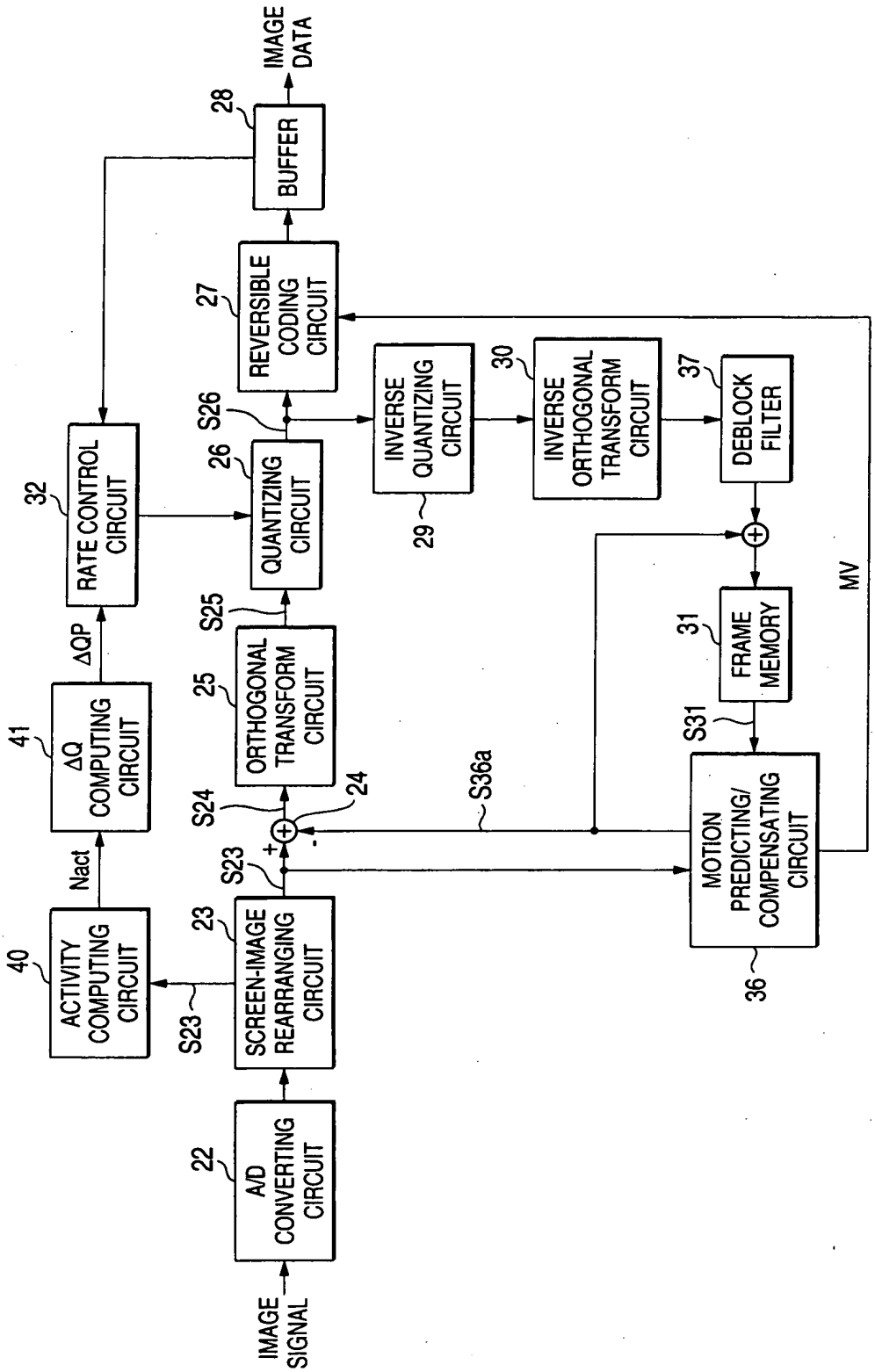
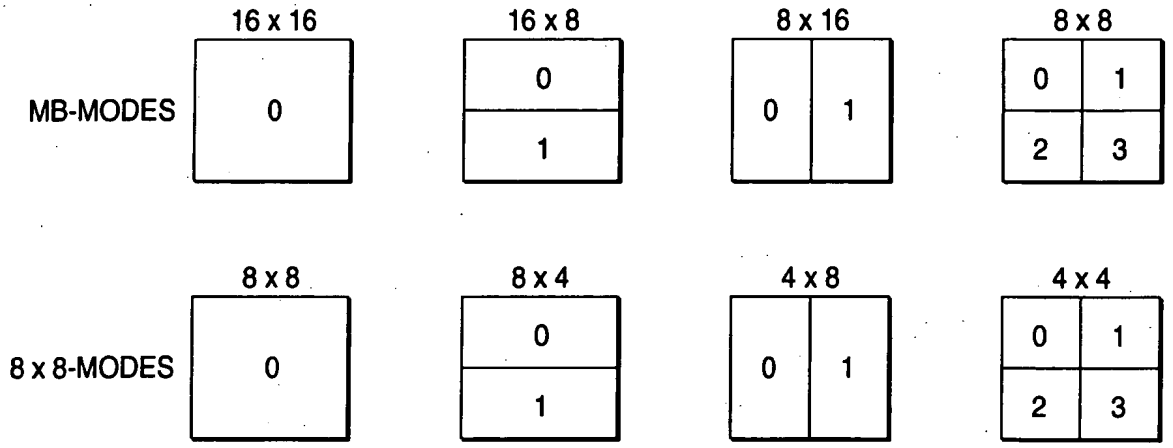

2
IMAGE SIGNAL
A/D CONVERTING CIRCUIT
22
SCREEN-IMAGE REARRANGING CIRCUIT
23
S23
ACTIVITY COMPUTING CIRCUIT
40
Nact
ΔQ COMPUTING CIRCUIT
41
ΔQP
RATE CONTROL CIRCUIT
32
S23
+
-
24
S24
ORTHOGONAL TRANSFORM CIRCUIT
25
S25
QUANTIZING CIRCUIT
26
S26
REVERSIBLE CODING CIRCUIT
27
BUFFER
28
IMAGE DATA
INVERSE QUANTIZING CIRCUIT
29
INVERSE ORTHOGONAL TRANSFORM CIRCUIT
30
DEBLOCK FILTER
37
FRAME MEMORY
31
S31
MOTION PREDICTING/ COMPENSATING CIRCUIT
36
S36a
MV

FIG. 11

80

INPUT: Nact		OUTPUT: ΔQP
MINIMUM VALUE	MAXIMUM VALUE	
0.5	0.536168	-6
0.536168	0.600508	-5
0.600508	0.672569	-4
0.672569	0.753277	-3
0.753277	0.843671	-2
0.843671	0.944911	-1
0.944911	1.058301	0
1.058301	1.185297	+1
1.185297	1.327532	+2
1.327532	1.486836	+3
1.486836	1.665256	+4
1.665256	1.865087	+5
1.856087	2.0	+6

FIG. 12


MB-MODES
16 x 16
0
16 x 8
0
1
8 x 16
0
1
8 x 8
0
1
2
3
8 x 8-MODES
8 x 8
0
8 x 4
0
1
4 x 8
0
1
4 x 4
0
1
2
3